THE INFLUENCE OF DEVICE GEOMETRY ON THE PARTIALLY DEPLETED SOI TRANSISTOR TID HARDNESS*

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Abstract. *The research is focused on the differences in radiation behavior for transistors of different geometry, body tie contact types, device layer thickness and biasing.*

Key words**:** *CMOS SOI, TID Hardness, automated measurement system, body tie.*

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1. INTRODUCTION

Silicon on Insulator (SOI) process grants several benefits as compared to bulk silicon substrate. Active devices are formed in the silicon layer placed on buried SiO_2 insulator layer. Fully isolated transistors have lower leakage current, less parasitic capacitance and therefore lower power consumption and higher switching speed.

SOI transistors can be fully and partially depleted. If the depletion region reaches buried oxide, the transistor is fully depleted, otherwise it is called partially depleted. Fully depleted transistors can control the channel more efficiently; however, they require precise thin silicon films, good process reproducibility and thus are more difficult to produce.

SOI process is successfully used in radiation hardness applications since the insulator layer reduces photocurrents and eliminates latch-up as a result of transient radiation effects (TRE) and single event effects (SEE).

At the same time SOI devices are relatively more vulnerable to total ionized dose (TID) effects because the buried oxide works like the gate oxide of the additional “bottom” transistor – parasitic structure specific to SOI process. Radiation induced threshold voltage shift of this structure leads to leakage current increase and can cause parametrical failure of the complex device due to increased current supply. Radiation hardness research of separate transistors can offer opportunity to evaluate complex devices’ hardness [1-11] or serve as the basis for the fundamental modeling of the separate transistor [5, 12-17].

On the other side, one can use body ties that increase device’s TID hardness mitigating parasitic bipolar effect [18]. Some benefits can be gained by careful transistor type and process parameters selection and suitable substrate biasing [19]. Prior theoretical conclusions on radiation hardness of SOI devices are difficult to draw, thus experiment needs to be carried out. Special set-up is needed to automatically measure single transistor parameters.

2. TEST HARDWARE AND SOFTWARE

The devices under test (DUT) were test chips containing mesa-isolated transistor structures of different gate length and width, body tie contacts and device layer thickness. The topologies of transistors are presented in figure 1.

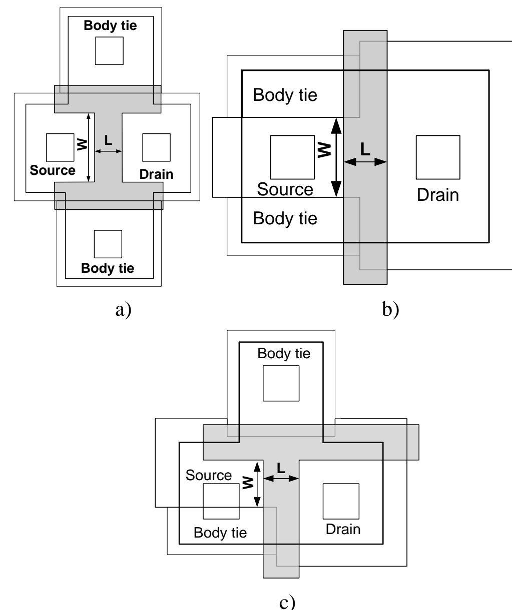

Figure 1. The topologies of transistors: a) H-type transistor: Body ties are located on the each side of transistor; b) L-type transistor: body is tied to source; c) T-type transistor: both external body contacts and body-tied-to-source blocks are presented.

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Gate oxide has a thickness of 12 nm and the buried oxide is 0.4 μm thick. Device cross section is presented in figure 2.

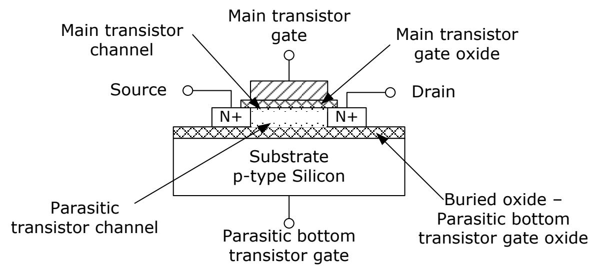

Figure 2. Cross section of NMOS transistor.

Test structures were irradiated under different bias conditions presented in Table 1.

Table 1. Transistor'sbias conditions under irradiation

Mode	Source	Drain	Main gate	Body	Bottom gate
ON	0	0	5	0	0
OFF	0	5	0	0	0
TG_0	5	5	0	0	0
TG_-2	5	5	0	0	-2

Measurement set-up was based on National Instruments equipment that gives us possibility to acquire sets of transistor I-V curves during irradiation. Drain current was measured by NI PXI-4071 digital multimeter which has a resolution down to 1 pA. Measurements were automatized by means of program developed in LabVIEW 2010. Hardware was controlled by program designed in LabVIEW 2010 development environment.TID test were carried out with ^{137}Cs MEPHI-SPELS facility and with "REIS-IE" X-ray tester [20]. The dose rate was 12 rad/sec.

3. Experimental Results

The radiation-induced threshold voltage shift behavior of the main (top) and bottom transistor depends on channel type and dimensions, gate shape, device layer thickness and bias conditions.

One should mention that parasitic bottom transistor I-V curves alteration under irradiation is noticeably higher than one of the main transistors. This experimental fact is illustrated by figures 3 and 4 for the case of NMOS H-type transistor with dimensions L=0.6 μm and W=1.4 μm irradiated under TG_0 bias conditions.

These figures correspond with the above mentioned fact that regards leakage current increase to parasitic bottom transistor radiation-induced threshold voltage shift.

It was found that short channel transistors have higher threshold voltage shift than long channel ones. That dependence was caused by different field distribution in the buried oxide for short and long-channel devices under the TG bias as was shown in [19]. For long gate, drain and source bias only enhance charge trapping in local areas around the source and drain, having little effect on the central area under the gate. Especially significant characteristic TID-degradation occurs in structures that combine short gate length and large gate width. Width dependence presumably is due to more significant effect of device edges on charge trapping in buried oxide area under the gate in narrow devices.

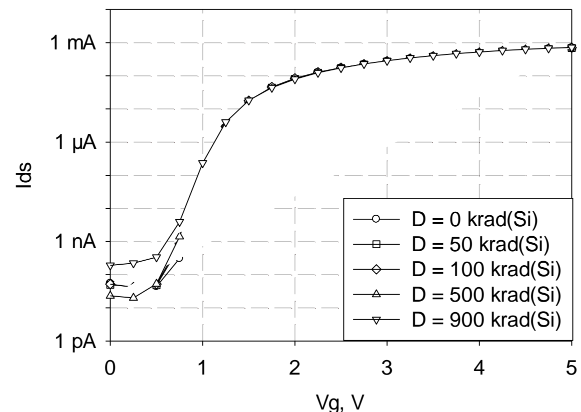

Figure 3. Dependence of main transistor drain-source current on gate voltage at various total ionizing doses.

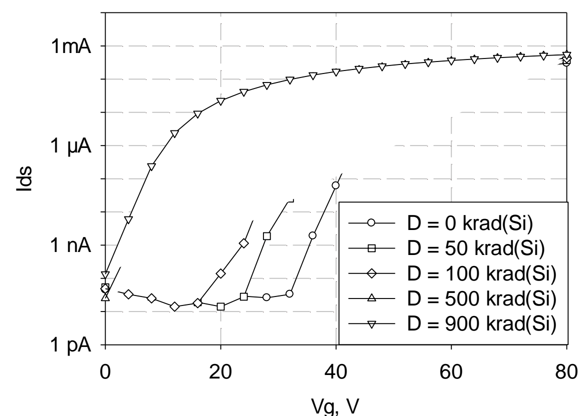

Figure 4. Dependence of bottom transistor drain-source current on gate voltage at various total ionizing doses.

Bottom transistor threshold voltage dependences on total ionizing dose for different transistor's channel length and width values and TG_0 bias during irradiation are shown in figure 5. Threshold voltage is measured as the voltage that corresponds to the current of 1 μA.

The same dependence evidently reveals itself on diagrams corresponding to L-type transistors of different channel dimensions presented in Figure 6. These were irradiated in OFF mode. One should mention that L-type transistors are not able to work

exactly in TG mode because of body-tied-to-source blocks.

The influence of bias conditions is interrelated to the transistor type. The most TID-sensitive bias conditions correspond with the “TG” bias mode. This effect is strongly pronounced for H-type transistors that have independent contacts to the body region. The worst bias case during irradiation for L-type transistors that include body-tied-to-source (BTS) blocks was “OFF”.

Device layer thickness influences the main transistor threshold voltage shift more significantly than one of the bottom transistor. Transistor structures made on the wafer with the thickest device layer demonstrated higher characteristic’s degradation as compared to transistors with lower device layer thickness.

The substrate was grounded in most cases. Negative offset voltage applied to the substrate reduces the threshold voltage shift.

Threshold voltages’ shifts of the bottom NMOS transistors are summarized on figures7-9for structures with various channel widths and lengths that were irradiated in various bias conditions.

T-type transistors combine features of H- and L-type transistors: they have both independent body contacts and body-tied to source blocks. Under ON and OFF bias conditions T-type transistors showed behavior similar to that of H- and L-type transistors of the same channel size.

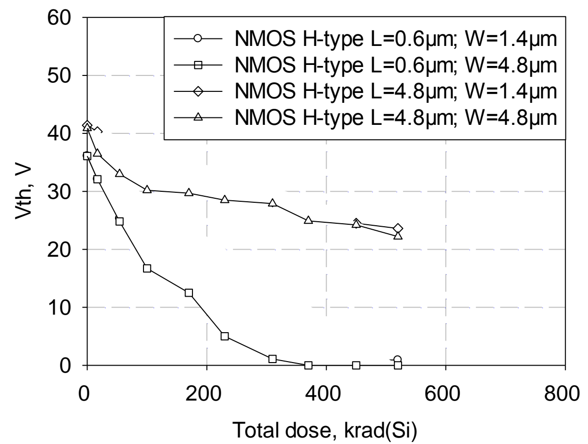

Figure 5. Dependence of bottom transistor drain-source current on total ionizing dose for different channel width and height.

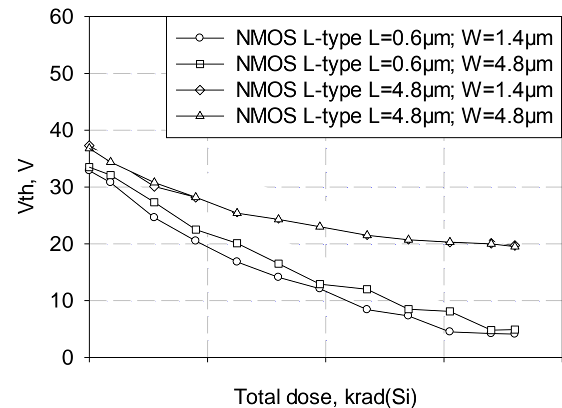

Figure 6. Dependence of bottom transistor drain-source current on total ionizing dose for different transistor channel width and height.

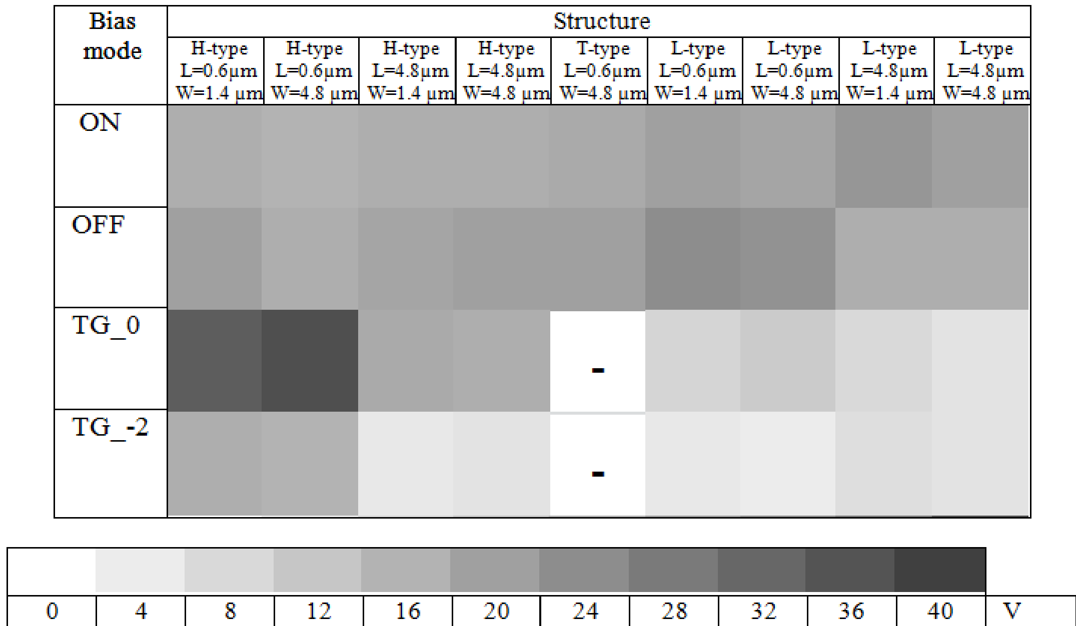

Figure 7. Threshold voltages' shifts of the bottom NMOS transistors for structures with different channel width and length. Device layer thickness is 0.2 µm.

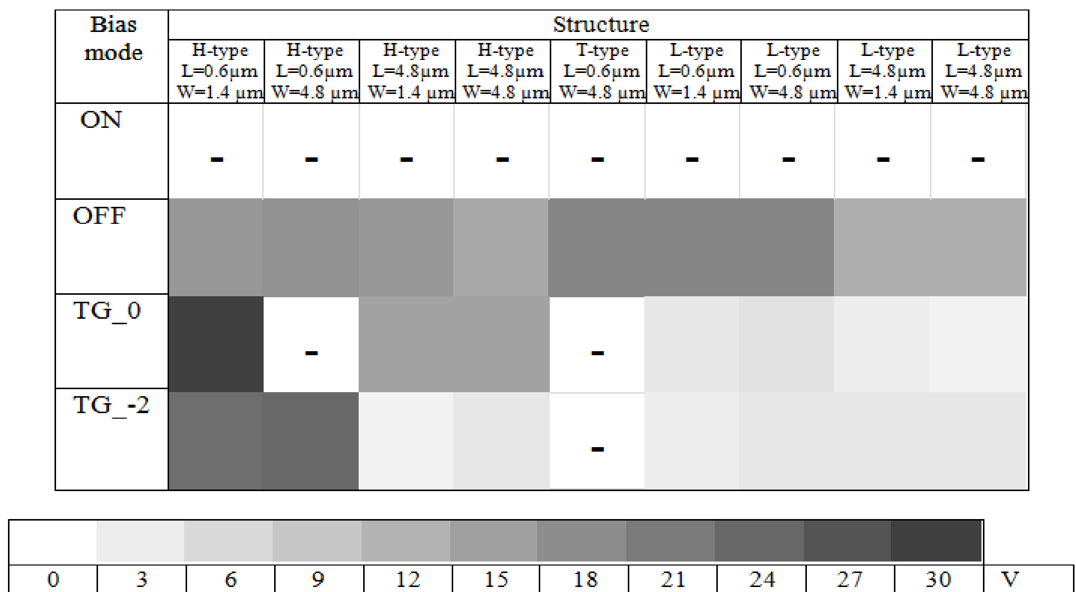

Figure 8. Threshold voltages' shifts of the bottom NMOS transistors for structures with different channel width and length. Device layer thickness is 0.14 µm.

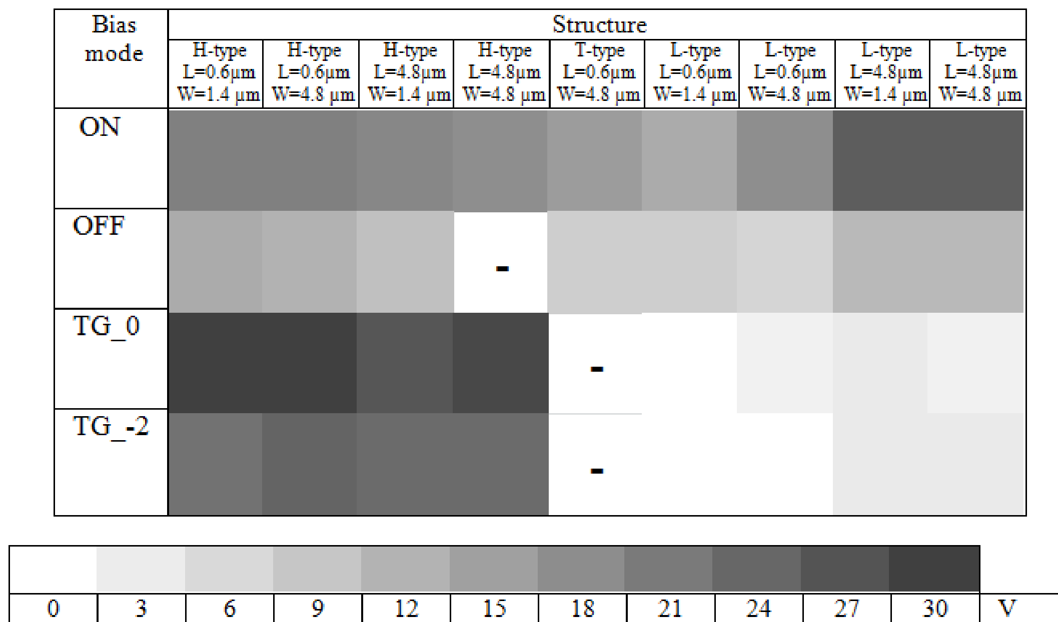

Figure 9. Threshold voltages' shifts of the bottom NMOS transistors for structures with different channel width and length. Device layer thickness is 0.3 µm.

4. Conclusion

The purpose of this paper was to estimate the influence of the device geometry on the partially depleted SOI transistors TID hardness. It was experimentally found out that TID-induced threshold voltage shifts are relatively higher for shorted and wider channels of test transistors and occur on lower dose. Transmission gate with ground potential applied to the substrate should be considered as the worst bias case.

The results can be used to determine the components of the complex IC that are most vulnerable to ionizing radiation based on analysis of used transistors' geometry and their biasing.

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